



R650X and R651X Microprocessors (CPU)

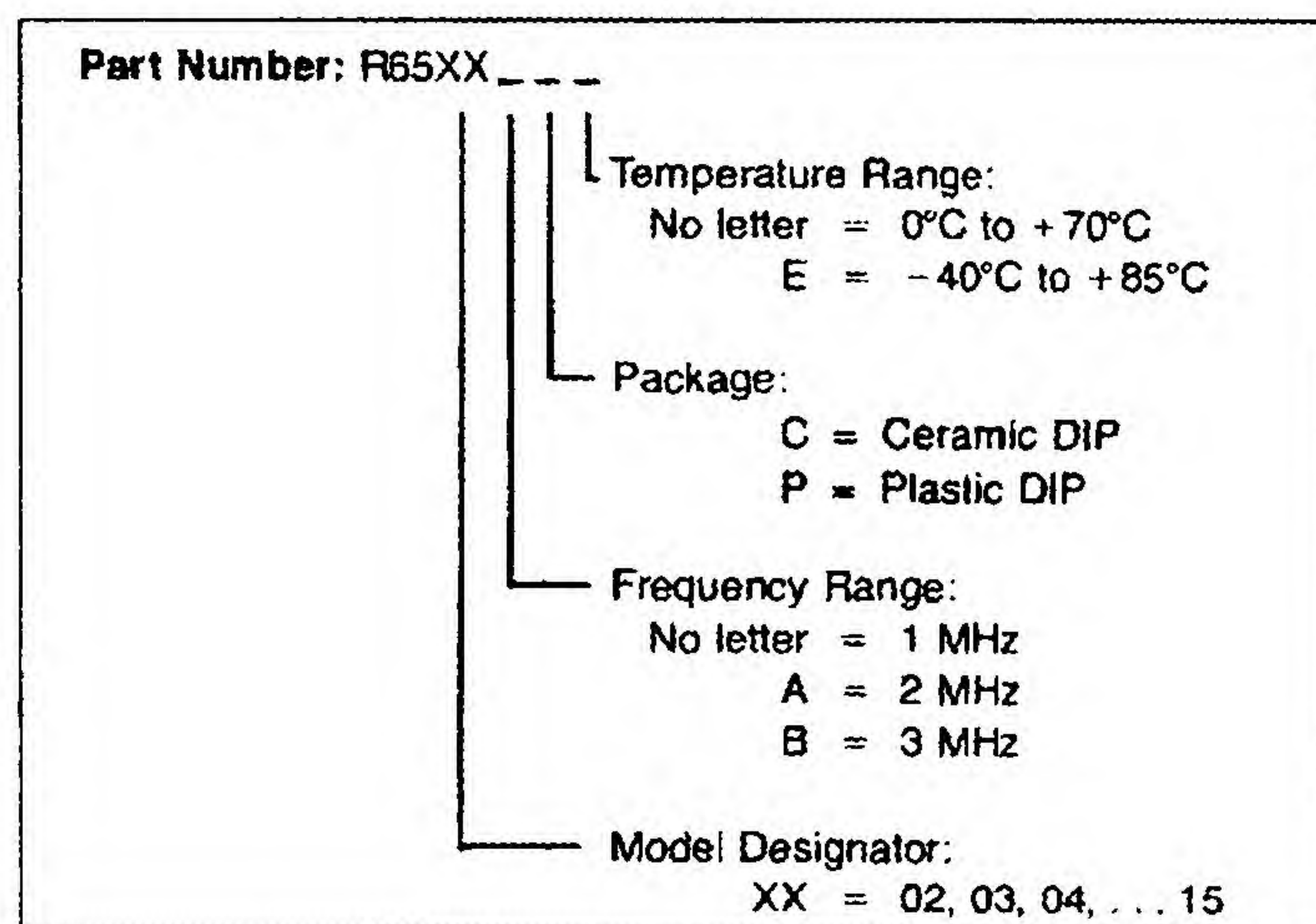
DESCRIPTION

The 8-bit R6500 microprocessor devices are produced with N-channel, silicon gate technology. Performance speeds are enhanced by advanced system architecture. This innovative architecture results in smaller chips—the semiconductor threshold is cost-effectivity. System cost-effectivity is further enhanced by providing a family of 10 software-compatible microprocessor (CPU) devices, described in this document. Rockwell also provides single chip microcomputers, memory and peripheral devices—as well as low-cost design aids and documentation.

Ten CPU devices are available. All are software-compatible. They provide options of addressable memory, interrupt input, on-chip clock oscillators and drivers. All are bus-compatible with earlier generation microprocessors like the M6800 devices.

The R650X and R651X family includes six microprocessors with on-board clock oscillators and drivers and four microprocessors driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single phase inputs, crystal or RC inputs provide the time base. The external clock versions are geared for multiprocessor system applications where maximum timing control is mandatory. All R6500 microprocessors are also available in a variety of packaging (ceramic and plastic), operating frequency (1 MHz, 2 MHz and 3 MHz) and temperature (commercial and industrial) versions.

ORDERING INFORMATION



FEATURES

- N-channel, silicon gate, depletion load technology
- 8-bit parallel processing
- 56 instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt request
- Non-maskable interrupt
- Use with any type of speed memory
- 8-bit bidirectional data bus
- Addressable memory range of up to 64K bytes
- "Ready" input
- Direct Memory Access capability
- Bus compatible with M6800
- 1 MHz, 2 MHz, and 3 MHz versions
- Choice of external or on-chip clocks
 - External single clock input
 - Crystal time base input
- Commercial and industrial temperature versions
- Pipeline architecture
- Single +5V supply

R6500 CPU FAMILY MEMBERS

Microprocessors with Internal Two Phase Clock Generator

Model	No. Pins	Addressable Memory
R6502	40	64K Bytes
R6503	28	4K Bytes
R6504	28	8K Bytes
R6505	28	4K Bytes
R6506	28	4K Bytes
R6507	28	8K Bytes

Microprocessors with External Two Phase Clock Input

Model	No. Pins	Addressable Memory
R6512	40	64K Bytes
R6513	28	4K Bytes
R6514	28	8K Bytes
R6515	28	4K Bytes

INTERFACE SIGNAL DESCRIPTIONS

CLOCKS ($\phi 1$, $\phi 2$)

The R651X requires a two phase non-overlapping clock that runs at the V_{CC} voltage level. The R650X clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled.

ADDRESS BUS (A0–A15)

The address line outputs access data in memory device locations or cells, access data in I/O device registers and/or effect logical operations in I/O or controller devices depending on system design. The addressing range is determined by the number of address lines available on the particular CPU device. The R6502 and R6512 can address 64K bytes with a 16-bit address bus (A0–A15); the R6504, R6507, and the R6514 can address 8K bytes with a 13-bit address bus (A0–A12); and the R6503, R6505, R6506, R6513, and R6515 can address 4K bytes with a 12-bit address bus (A0–A11). These outputs are TTL-compatible and are capable of driving one standard TTL load and 130 pF.

DATA BUS (D0–D7)

The data lines (D0–D7) form an 8-bit bidirectional data bus which transfers data between the CPU and memory or peripheral devices. The outputs are tri-state buffers capable of driving one standard TTL load and 130 pF.

DATA BUS ENABLE (DBE, R6512 ONLY)

The TTL-compatible DBE input allows external control of the tri-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation DBE is driven by the phase two ($\phi 2$) clock, thus allowing data output from microprocessor only during $\phi 2$. During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally, DBE should be held low.

READY (RDY)

The Ready input signal allows the user to halt or single cycle the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with phase one ($\phi 1$) will halt the microprocessor with the output address lines reflecting the current address being fetched. If Ready is low during a write cycle, it is ignored until the following read operation. This condition will remain through a subsequent phase two ($\phi 2$) in which the Ready signal is low. This feature allows microprocessor interfacing with the low speed PROMs as well as Direct Memory Access (DMA).

INTERRUPT REQUEST (\overline{IRQ})

The TTL level active-low \overline{IRQ} input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Processor Status Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register

are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts can occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3K Ω external resistor should be used for proper wire-OR operation.

NON-MASKABLE INTERRUPT (\overline{NMI})

A negative going edge on the \overline{NMI} input requests that a non-maskable interrupt sequence be generated within the microprocessor.

\overline{NMI} is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for \overline{IRQ} will be performed, regardless of the state interrupt mask flag. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.

\overline{NMI} also requires an external 3K Ω resistor to V_{CC} for proper wire-OR operations.

Inputs \overline{IRQ} and \overline{NMI} are hardware interrupts lines that are sampled during $\phi 2$ (phase 2) and will begin the appropriate interrupt routine on the $\phi 1$ (phase 1) following the completion of the current instruction.

SET OVERFLOW FLAG (\overline{SO})

A negative going edge on the \overline{SO} input sets the overflow bit in the Processor Status Register. This signal is sampled on the trailing edge of $\phi 1$ and must be externally synchronized.

SYNC

The SYNC output line identifies those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during $\phi 1$ of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the $\phi 1$ clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

RESET (\overline{RES})

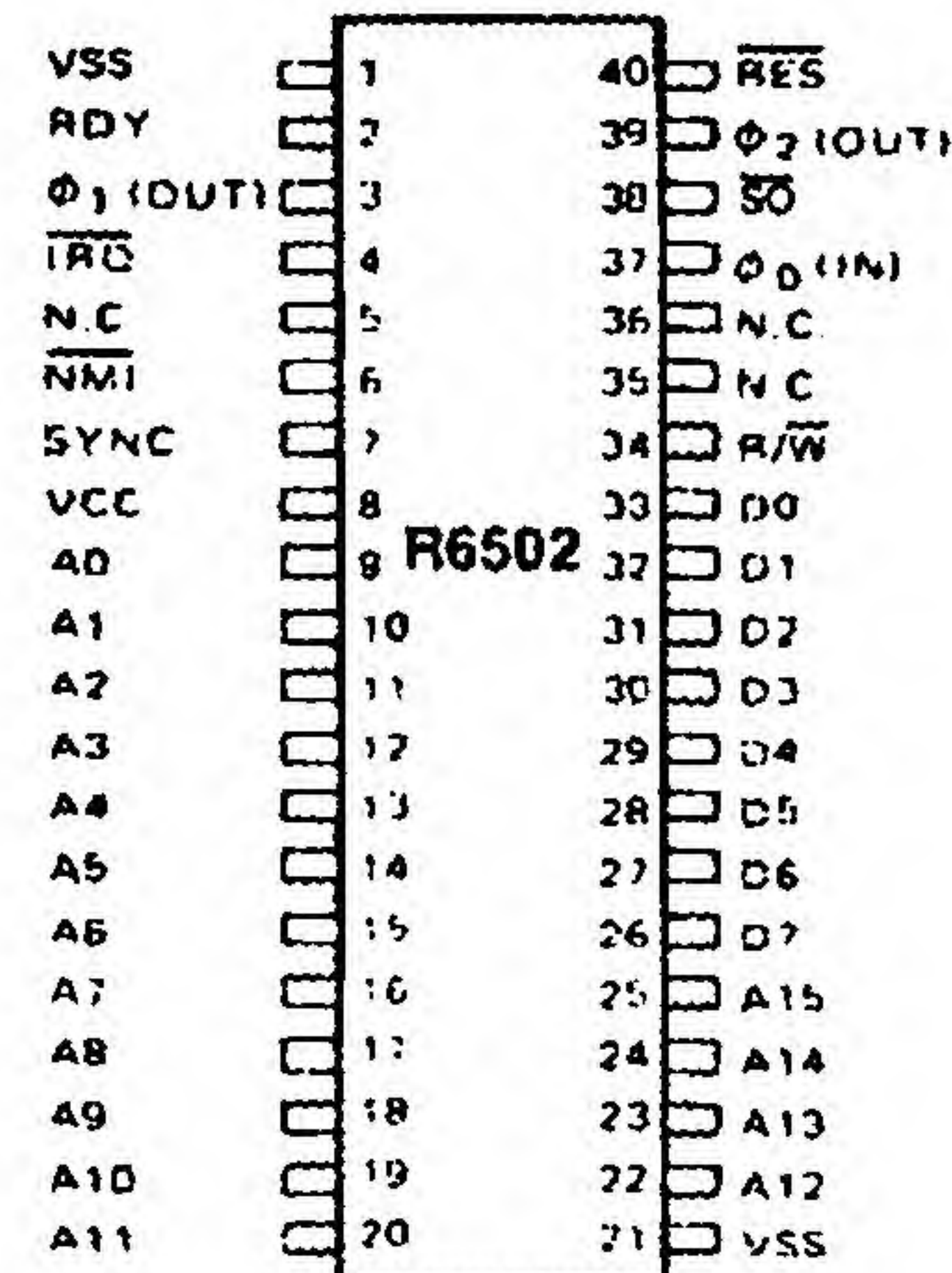
The active low \overline{RES} resets, or starts, the microprocessor from a power down or restart condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag is set and the microprocessor loads the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

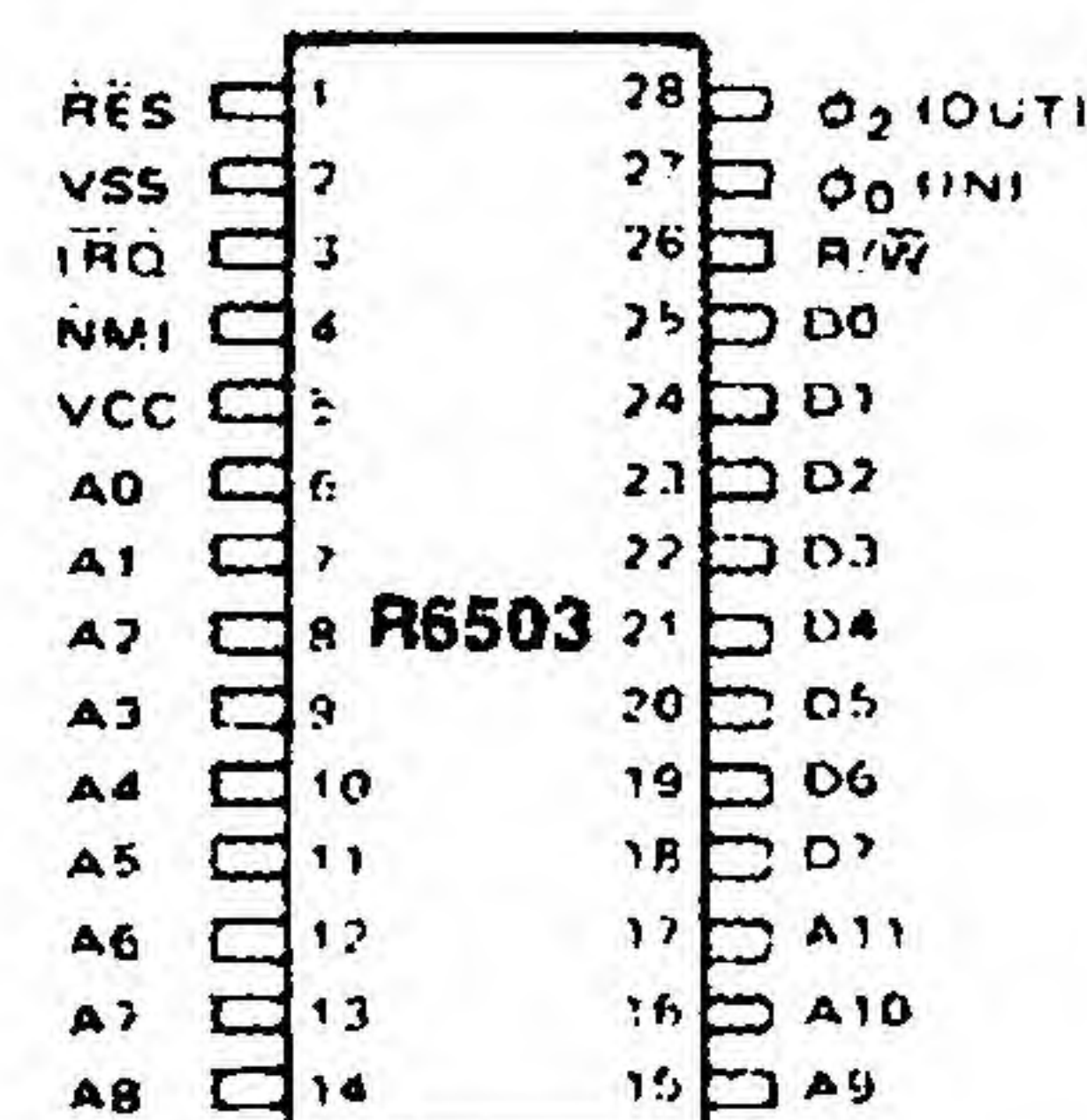
After V_{CC} reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/W and SYNC signals become valid.

R6502 FEATURES

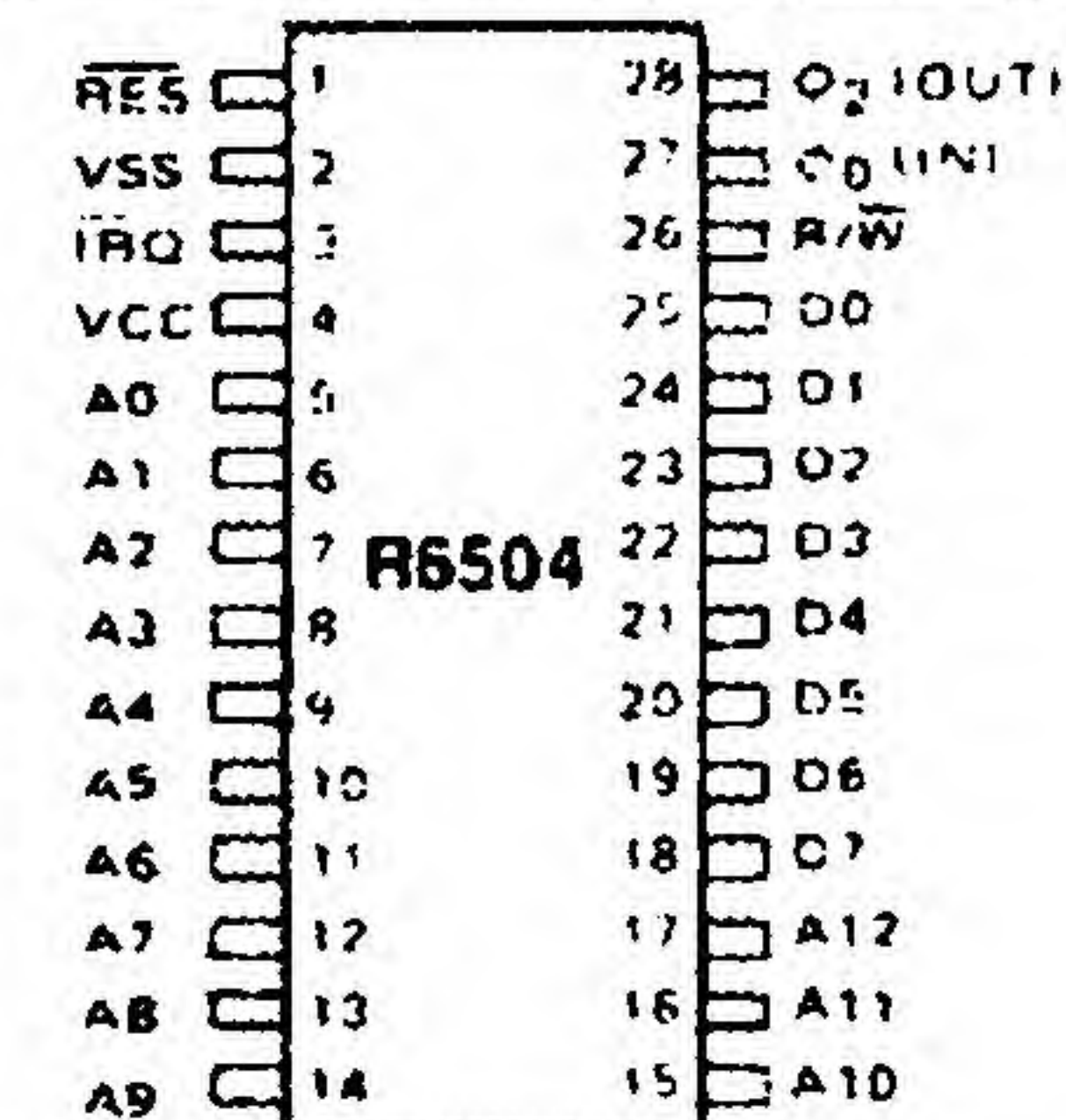
- 64K addressable bytes of memory (A0-A15)
- On-chip clock
 - TTL-level single phase input
 - RC time base input
 - crystal time base input
- Two phase output clock for timing of support chips
- $\overline{\text{IRQ}}$ interrupt
- $\overline{\text{NMI}}$ interrupt
- RDY signal
- SYNC signal
(can be used for single instruction execution)
- 40-pin DIP

**R6503 FEATURES**

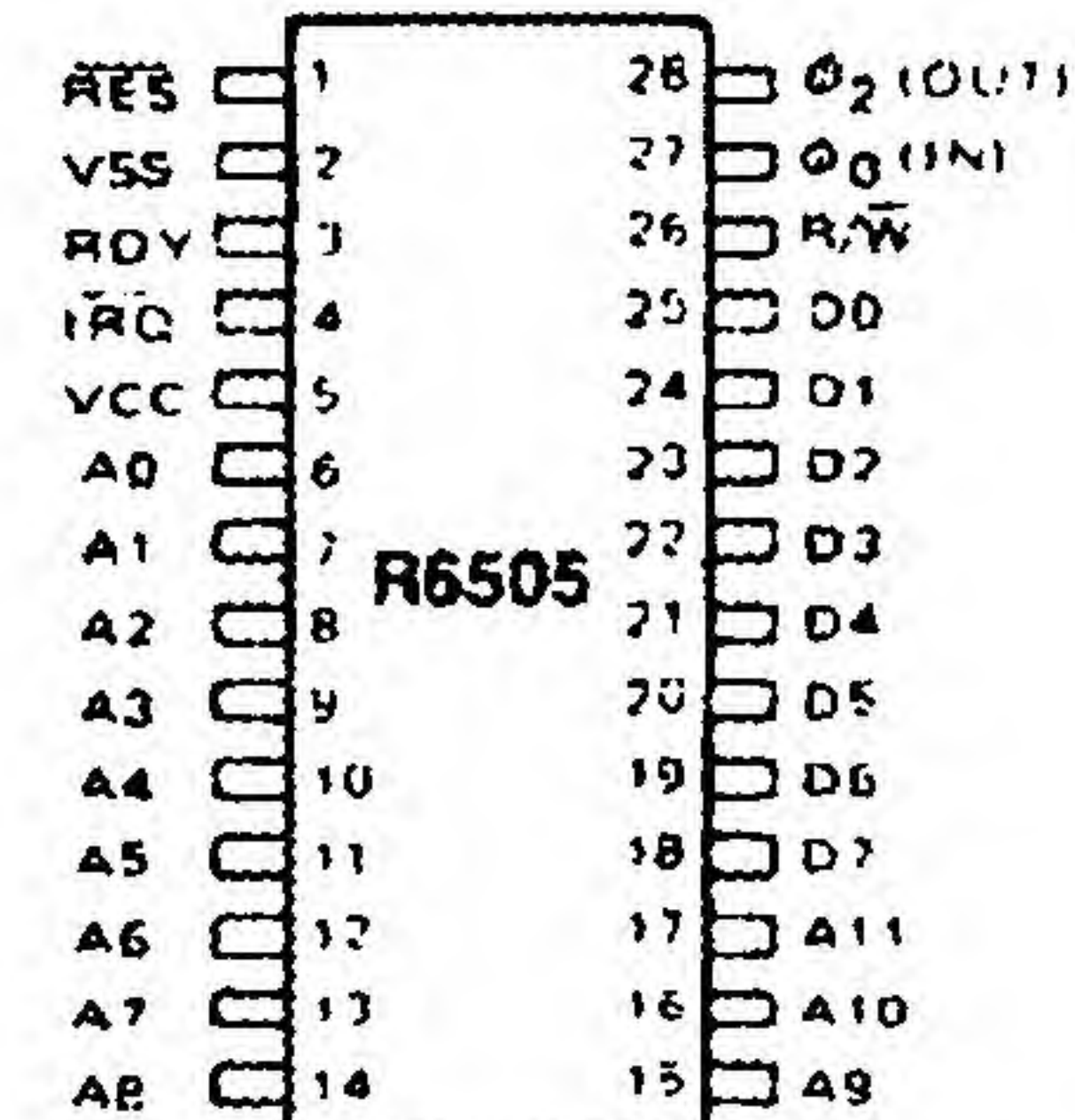
- 4K addressable bytes of memory (A0-A11)
- On-chip clock
- $\overline{\text{IRQ}}$ interrupt
- $\overline{\text{NMI}}$ interrupt
- 28-pin DIP

**R6504 FEATURES**

- 8K addressable bytes of memory (A0-A12)
- On-chip clock
- $\overline{\text{IRQ}}$ interrupt
- 28-pin DIP

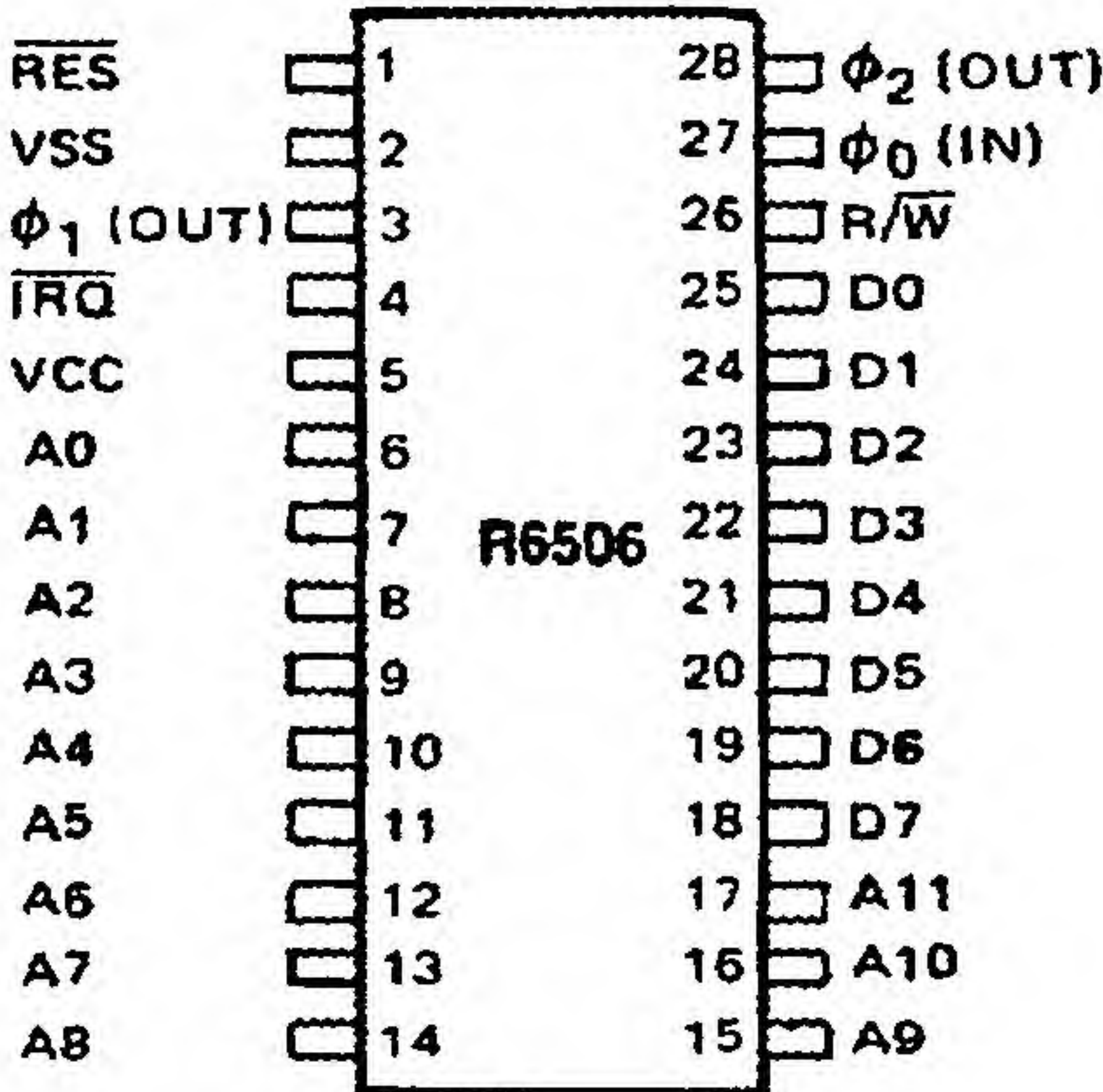
**R6505 FEATURES**

- 4K addressable bytes of memory (A0-A11)
- On-chip clock
- $\overline{\text{IRQ}}$ interrupt
- RDY signal
- 28-pin DIP



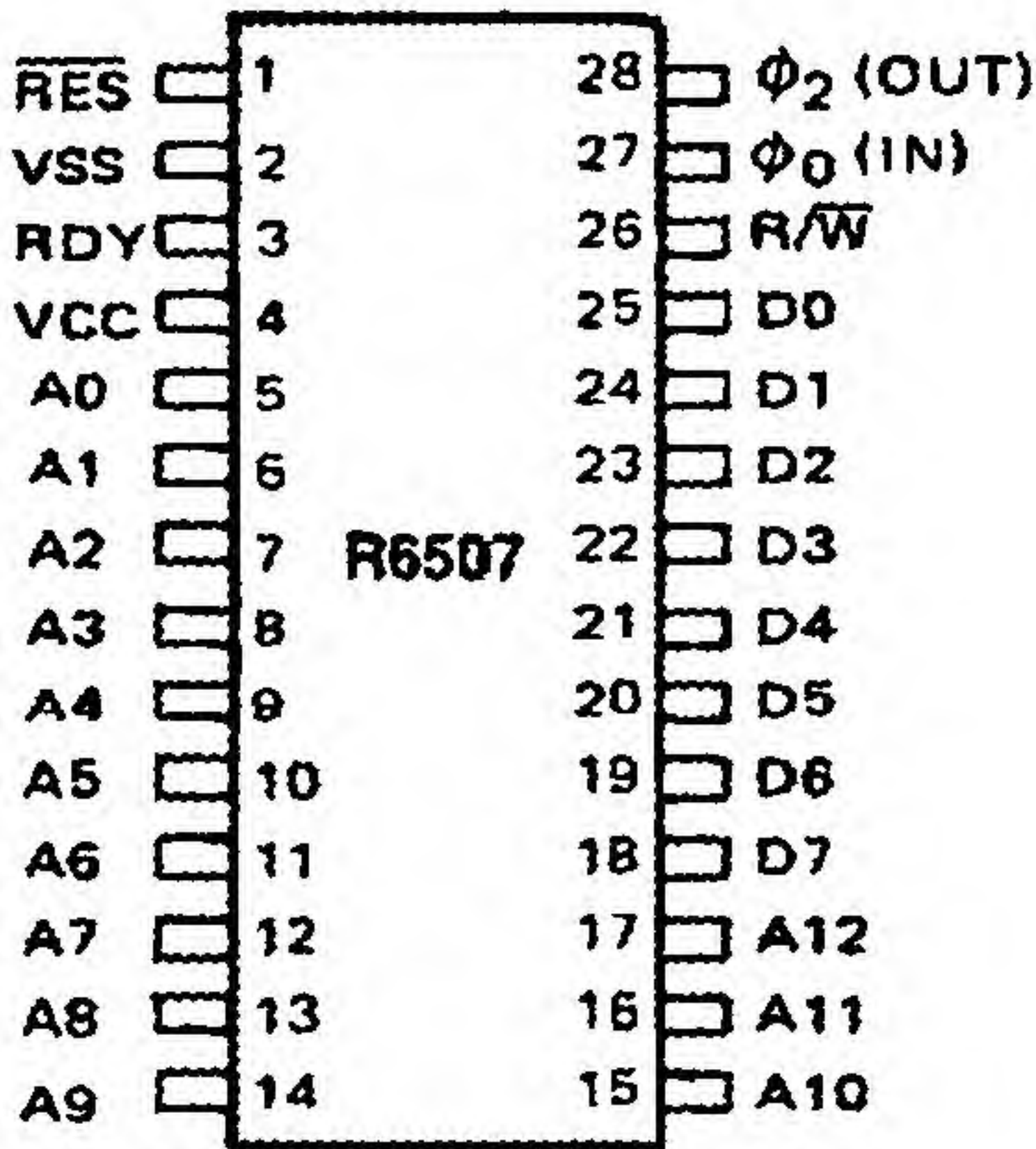
R6506 FEATURES

- 4K addressable bytes of memory (A0–A11)
- On-chip clock
- Two phase output clock for timing of support chips
- $\overline{\text{IRQ}}$ interrupt
- 28-pin DIP



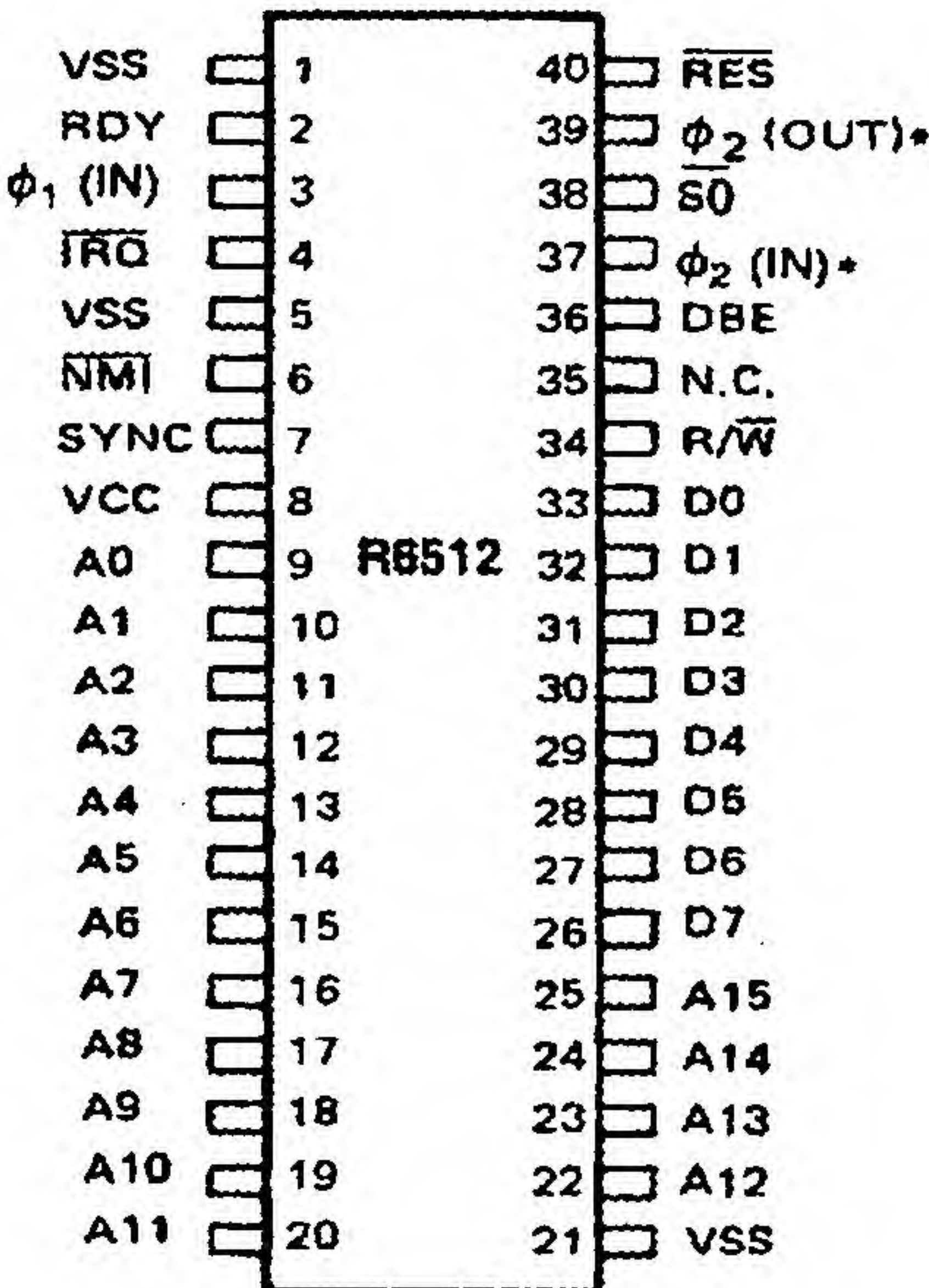
R6507 FEATURES

- 8K addressable bytes of memory (A0–A12)
- On-chip clock
- RDY signal
- 28-pin DIP



R6512 FEATURES

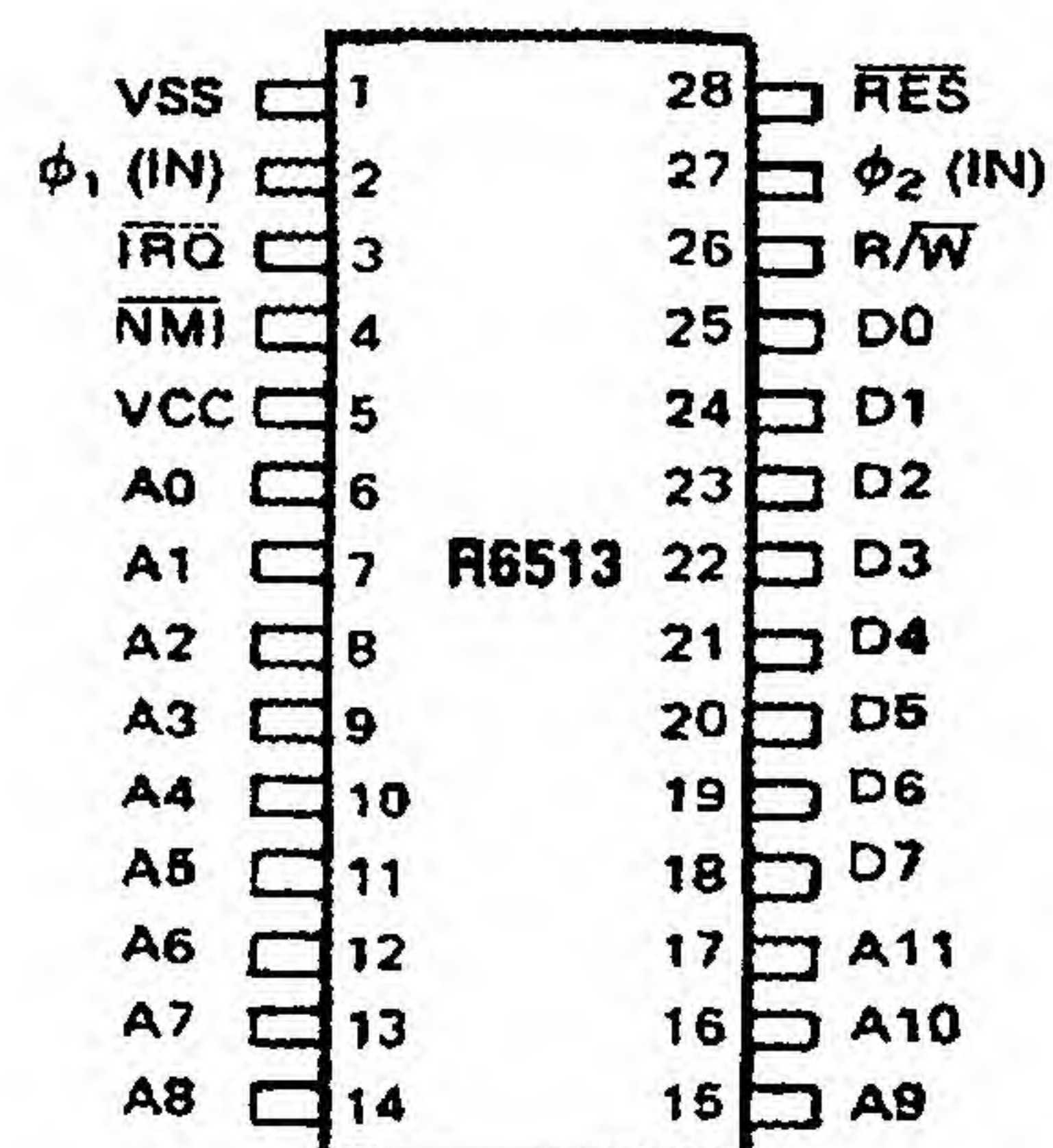
- 64K addressable bytes of memory (A0–A15)
- Two phase clock input
- $\overline{\text{IRQ}}$ interrupt
- NMI interrupt
- RDY signal
- SYNC signal
- Data Bus Enable
- 40-pin DIP



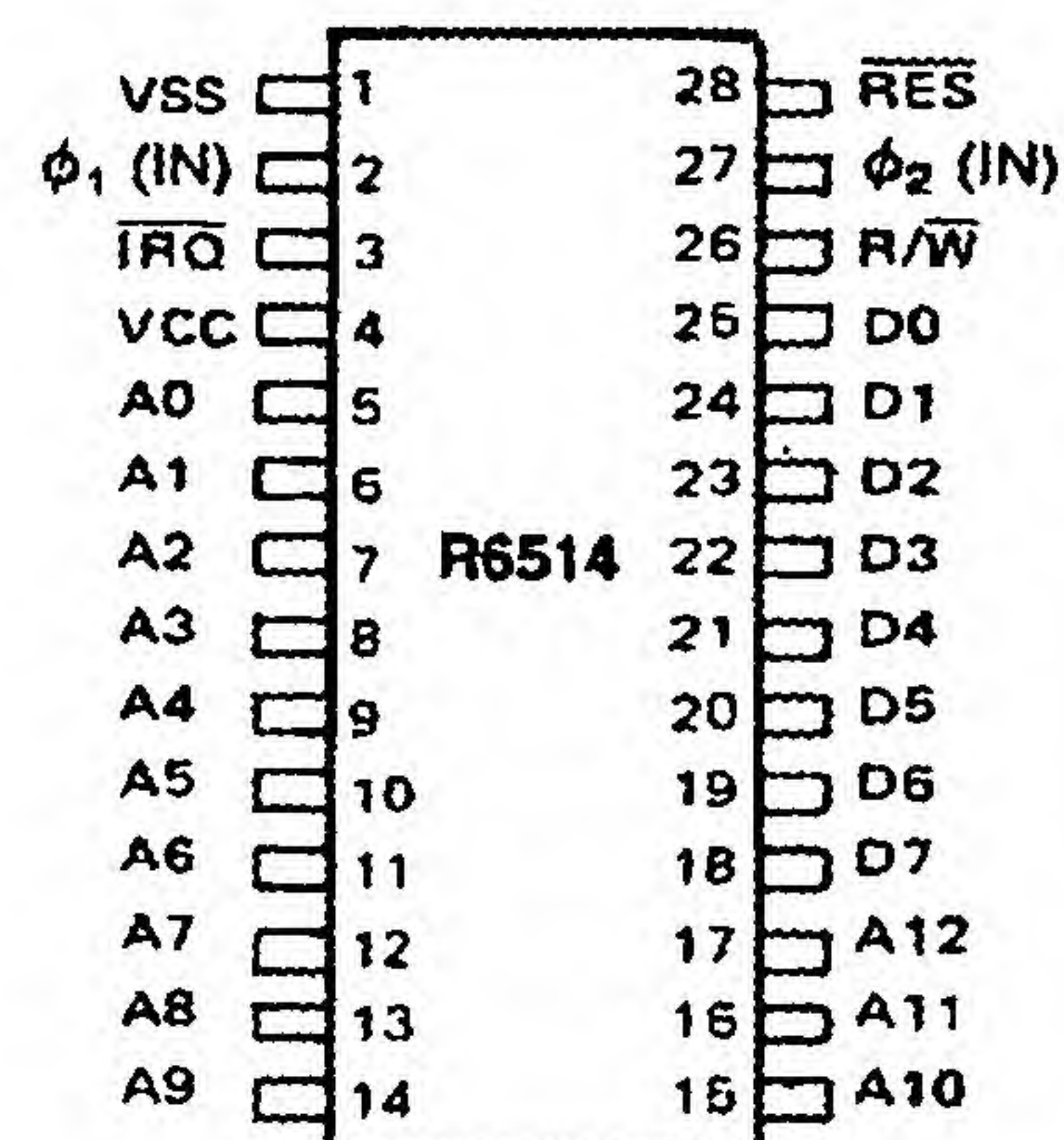
*Pins 37 and 39 are connected internally

R6513 FEATURES

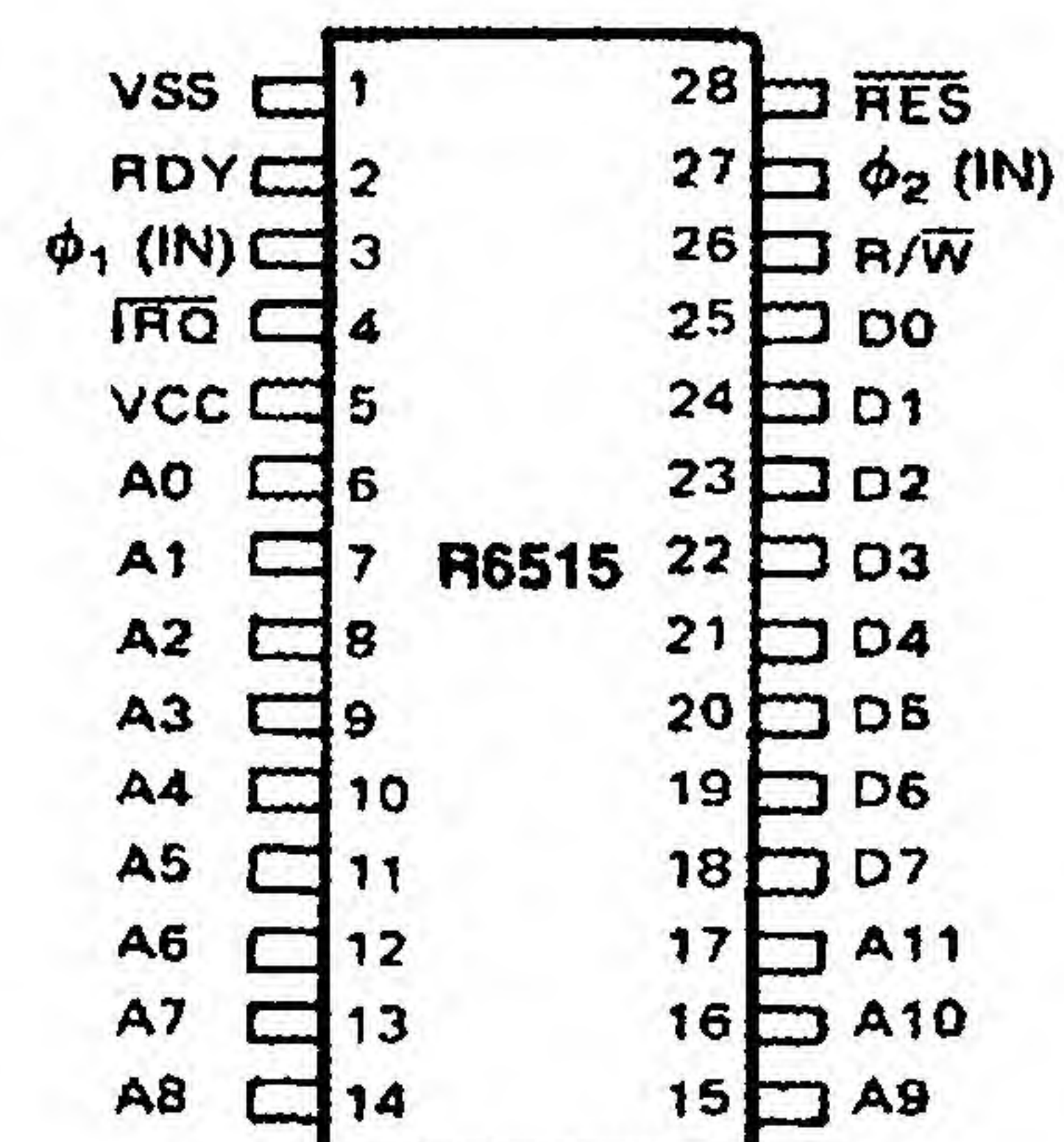
- 4K addressable bytes of memory (A0-A11)
- Two phase clock input
- $\overline{\text{IRQ}}$ interrupt
- $\overline{\text{NMI}}$ interrupt
- 28-pin DIP

**R6514 FEATURES**

- 8K addressable bytes of memory (A0-A12)
- Two phase clock input
- $\overline{\text{IRQ}}$ interrupt
- 28-pin DIP

**R6515 FEATURES**

- 4K addressable bytes of memory (A0-A11)
- Two phase clock input
- $\overline{\text{IRQ}}$ interrupt
- RDY signal
- 28-pin DIP



FUNCTIONAL DESCRIPTION

The internal organization of all R6500 CPUs is identical except for some variations in clock interface, the number of address output lines, and some unique input/output lines between versions.

CLOCK GENERATOR

The clock generator develops all internal clock signals, and (where applicable) external clock signals, associated with the device. It is the clock generator that drives the timing control unit and the external timing for slave mode operations.

TIMING CONTROL

The timing control unit keeps track of the instruction cycle being monitored. The unit is set to zero each time an instruction fetch is executed and is advanced at the beginning of each phase one clock pulse for as many cycles as is required to complete the instruction. Each data transfer which takes place between the registers depends upon decoding the contents of both the instruction register and the timing control unit.

PROGRAM COUNTER

The 16-bit program counter provides the addresses which step the microprocessor through sequential instructions in a program.

Each time the microprocessor fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

INSTRUCTION REGISTER AND DECODE

Instructions fetched from memory are gated onto the internal data bus. These instructions are latched into the instruction register, then decoded, along with timing and interrupt signals, to generate control signals for the various registers.

ARITHMETIC AND LOGIC UNIT (ALU)

All arithmetic and logic operations take place in the ALU including incrementing and decrementing internal registers (except the program counter). The ALU has no internal memory and is used only to perform logical and transient numerical operations.

ACCUMULATOR

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations, and in addition, the accumulator usually contains one of the two data words used in these operations.

INDEX REGISTERS

There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address.

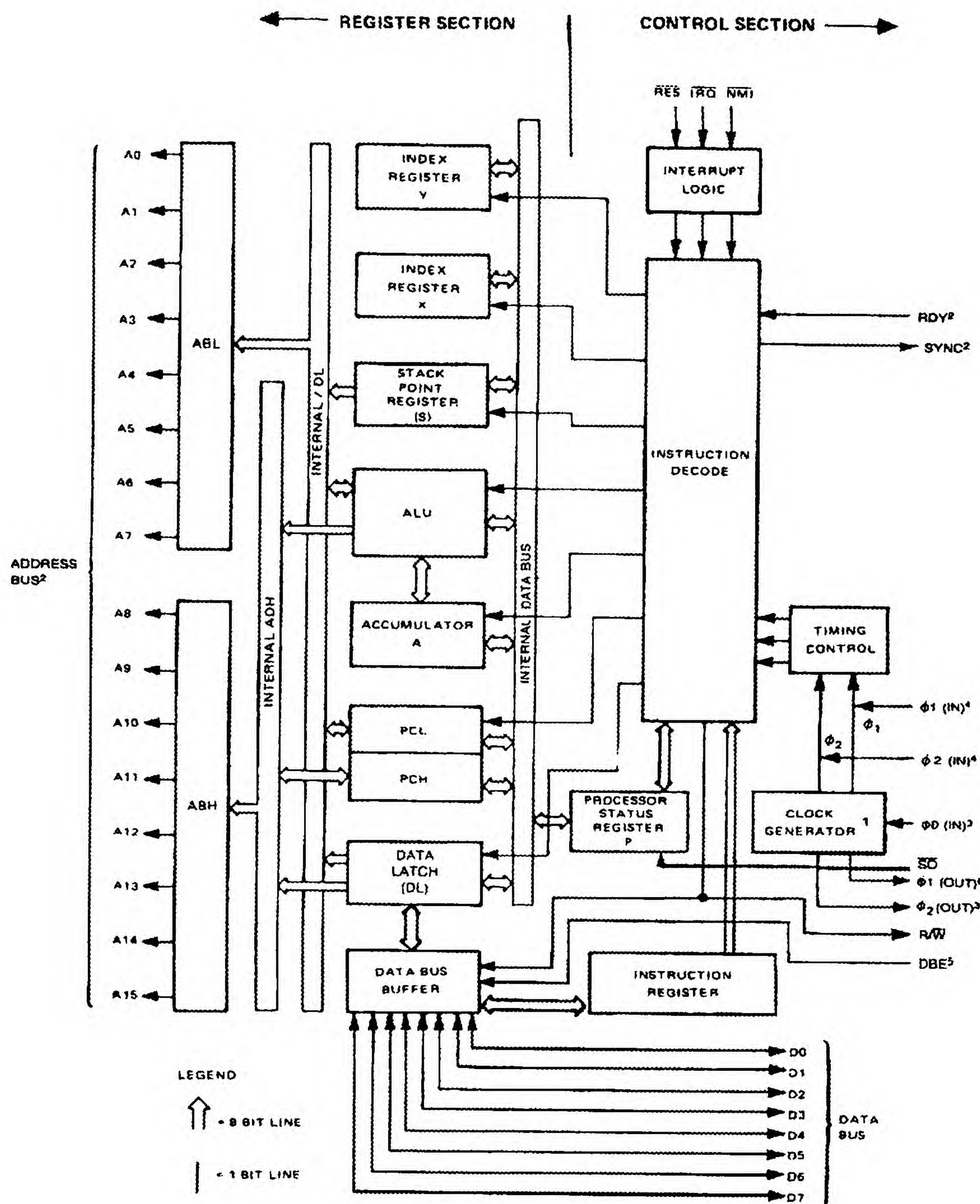
When executing an instruction which specifies indexed addressing, the CPU fetches the op code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-indexing of indirect addresses is possible (see addressing modes).

STACK POINTER

The stack pointer is an 8-bit register used to control the addressing of the variable-length stack on page one. The stack pointer is automatically incremented and decremented under control of the microprocessor to perform stack manipulations under direction of either the program or interrupts ($\overline{\text{NMI}}$ and $\overline{\text{IRQ}}$). The stack allows simple implementation of nested subroutines and multiple level interrupts. The stack pointer should be initialized before any interrupts or stack operations occur.

PROCESSOR STATUS REGISTER

The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both by the program and the CPU.



NOTE

1. CLOCK GENERATOR IS NOT INCLUDED ON R6512, R6513, R6514 AND R6515.
2. ADDRESSING CAPABILITY AND CONTROL OPTIONS VARY WITH EACH OF THE CPUs.
3. R6502, R6503, R6504, R6505, R6506 AND R6507.
4. R6512, R6513, R6514 AND R6515.
5. R6512 ONLY.
6. R6502 AND R6506.

R650X and R651X Internal Architecture

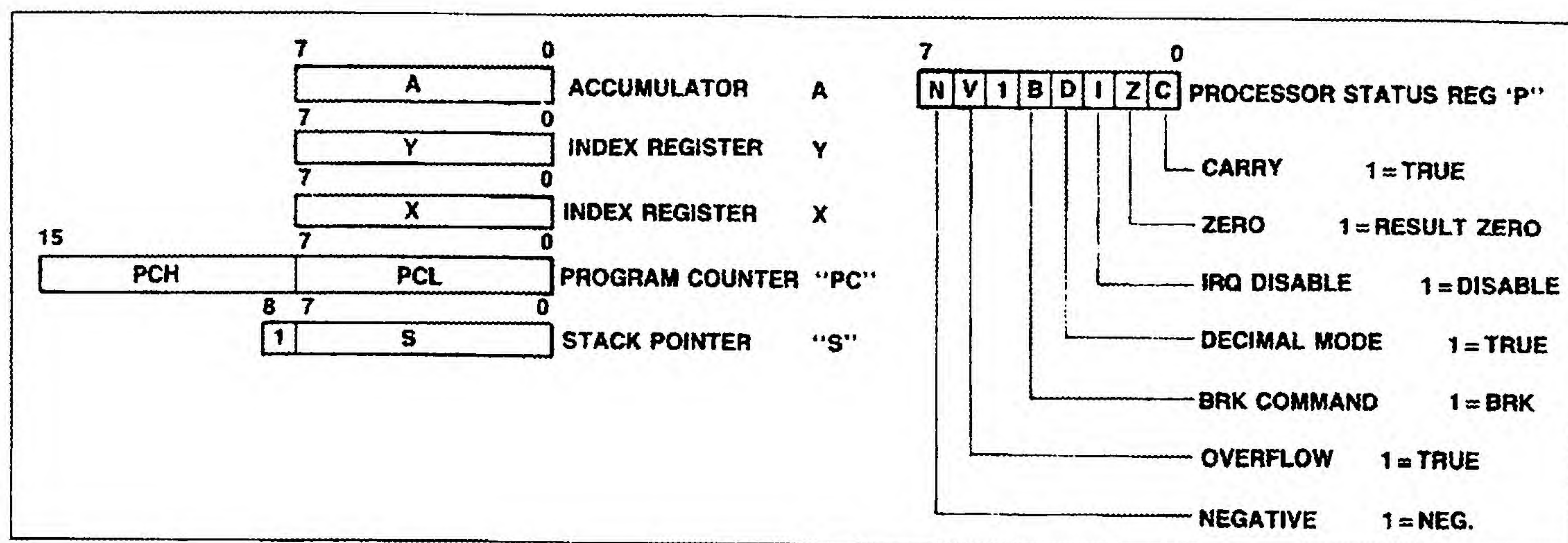
INSTRUCTION SET

The R6500 CPU has 56 instruction types which are enhanced by up to 13 addressing modes for each instruction. The

Accumulator, index registers, Program Counter, Stack Pointer and Processor Status Register are illustrated below.

Alphabetic Listing of Instruction Set

Mnemonic	Function	Mnemonic	Function
ADC	Add Memory to Accumulator with Carry	JMP	Jump to New Location
AND	"AND" Memory with Accumulator	JSR	Jump to New Location Saving Return Address
ASL	Shift Left One Bit (Memory or Accumulator)	LDA	Load Accumulator with Memory
BCC	Branch on Carry Clear	LDX	Load Index X with Memory
BCS	Branch on Carry Set	LDY	Load Index Y with Memory
BEQ	Branch on Result Zero	LSR	Shift One Bit Right (Memory or Accumulator)
BIT	Test Bits in Memory with Accumulator	NOP	No Operation
BMI	Branch on Result Minus	ORA	"OR" Memory with Accumulator
BNE	Branch on Result not Zero	PHA	Push Accumulator on Stack
BPL	Branch on Result Plus	PHP	Push Processor Status on Stack
BRK	Force Break	PLA	Pull Accumulator from Stack
BVC	Branch on Overflow Clear	PLP	Pull Processor Status from Stack
BVS	Branch on Overflow Set	ROL	Rotate One Bit Left (Memory or Accumulator)
CLC	Clear Carry Flag	ROR	Rotate One Bit Right (Memory or Accumulator)
CLD	Clear Decimal Mode	RTI	Return from Interrupt
CLI	Clear Interrupt Disable Bit	RTS	Return from Subroutine
CLV	Clear Overflow Flag	SBC	Subtract Memory from Accumulator with Borrow
CMP	Compare Memory and Accumulator	SEC	Set Carry Flag
CPX	Compare Memory and Index X	SED	Set Decimal Mode
CPY	Compare Memory and Index Y	SEI	Set Interrupt Disable Status
DEC	Decrement Memory by One	STA	Store Accumulator in Memory
DEX	Decrement Index X by One	STX	Store Index X in Memory
DEY	Decrement Index Y by One	STY	Store Index Y in Memory
EOR	"Exclusive-OR" Memory with Accumulator	TAX	Transfer Accumulator to Index X
INC	Increment Memory by One	TAY	Transfer Accumulator to Index Y
INX	Increment Index X by One	TSX	Transfer Stack Pointer to Index X
INY	Increment Index Y by One	TXA	Transfer Index X to Accumulator
		TXS	Transfer Index X to Stack Register
		TYA	Transfer Index Y to Accumulator



Programming Model

ADDRESSING MODES

The R6500 CPU family has 13 addressing modes. In the following discussion of these addressing modes, a bracketed expression follows the title of the mode. This expression is the term used in the Instruction Set Op Code Matrix table (later in this product description) to make it easier to identify the actual addressing mode used by the instruction.

ACCUMULATOR ADDRESSING [Accum]—This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESS [IMM]—In immediate addressing, the second byte of the instruction contains the operand, with no further memory addressing required.

ABSOLUTE ADDRESSING [Absolute]—In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 64K bytes of addressable memory.

ZERO PAGE ADDRESSING [ZP]—The zero page instructions allow for shorter code and execution times by fetching only the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

INDEXED ZERO PAGE ADDRESSING [ZP, X or Y]—This form of addressing is used with the index register and is referred to as "Zero Page, X" or "Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high order eight bits of memory and crossing of page boundaries does not occur.

INDEXED ABSOLUTE ADDRESSING [ABS, X or Y]—This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X" and "Absolute, Y." The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base

address. This type of indexing allows referencing of any location and the index may modify multiple fields, resulting in reduced coding and execution time.

IMPLIED ADDRESSING [Implied]—In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING [Relative]—Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction is an operand. This operand is an offset which is added to the program counter when the counter is set at the next instruction. The range of the offset is -128 to +127 bytes.

INDEXED INDIRECT ADDRESSING [(IND, X)]—In indexed indirect addressing (referred to as (Indirect, X)), the second byte of the instruction is added to the contents of index register X discarding the carry. The result of this addition points to a memory location on page zero which contains the low order byte of the effective address. The next memory location in page zero contains the high order byte of the effective address. Both memory locations specifying the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING [(IND), Y]—In indirect indexed addressing (referred to as (Indirect), Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location are added to the contents of index register Y. The result is the low order byte of the effective address. The carry from this addition is added to the contents of the next page zero memory location, to form the high order byte of the effective address.

ABSOLUTE INDIRECT [Indirect]—The second byte of the instruction contains the low order byte of a memory location. The high order eight bits of that memory location are contained in the third byte of the instruction. The contents of the fully specified memory location are the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter. (JMP (IND) only)

INSTRUCTION SET OP CODE MATRIX

The following matrix shows the Op Codes associated with the R6500 family of CPU devices. The matrix identifies the hexadecimal code, the mnemonic code, the addressing mode, the

number of instruction bytes, and the number of machine cycles associated with each Op Code. Also, refer to the instruction set summary for additional information on these Op Codes.

MSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5		PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6	
1	BPL Relative 2 2**	ORA (IND), Y 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6		CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7	
2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5		PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	
3	BMI Relative 2 2**	AND (IND), Y 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6		SEC Implied 1 2	AND ABS, Y 3 4*				AND ABS, X 3 4*	ROL ABS, X 3 7	
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5		PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	
5	BVC Relative 2 2**	EOR (IND), Y 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6		CLI Implied 1 2	EOR ABS, Y 3 4*				EOR ABS, X 3 4*	LSR ABS, X 3 7	
6	RTS Implied 1 6	ADC (IND, X) 2 6				ADC ZP 2 3	ROR ZP 2 5		PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6	
7	BVS Relative 2 2**	ADC (IND), Y 2 5*				ADC ZP, X 2 4	ROR ZP, X 2 6		SEI Implied 1 2	ADC ABS, Y 3 4*				ADC ABS, X 3 4*	ROR ABS, X 3 7	
8		STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3		DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	
9	BCC Relative 2 2**	STA (IND), Y 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4		TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5		
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3		TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	
B	BCS Relative 2 2**	LDA (IND), Y 2 5*			LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4		CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5		INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	
D	BNE Relative 2 2**	CMP (IND), Y 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6		CLD Implied 1 2	CMP ABS, Y 3 4*				CMP ABS, X 3 4*	DEC ABS, X 3 7	
E	CPX IMM 2 2	SBC (IND, X) 2 6			CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5		INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6	
F	BEO Relative 2 2**	SBC (IND), Y 2 5*				SBC ZP, X 2 4	INC ZP, X 2 6		SED Implied 1 2	SBC ABS, Y 3 4*				SBC ABS, X 3 4*	INC ABS, X 3 7	

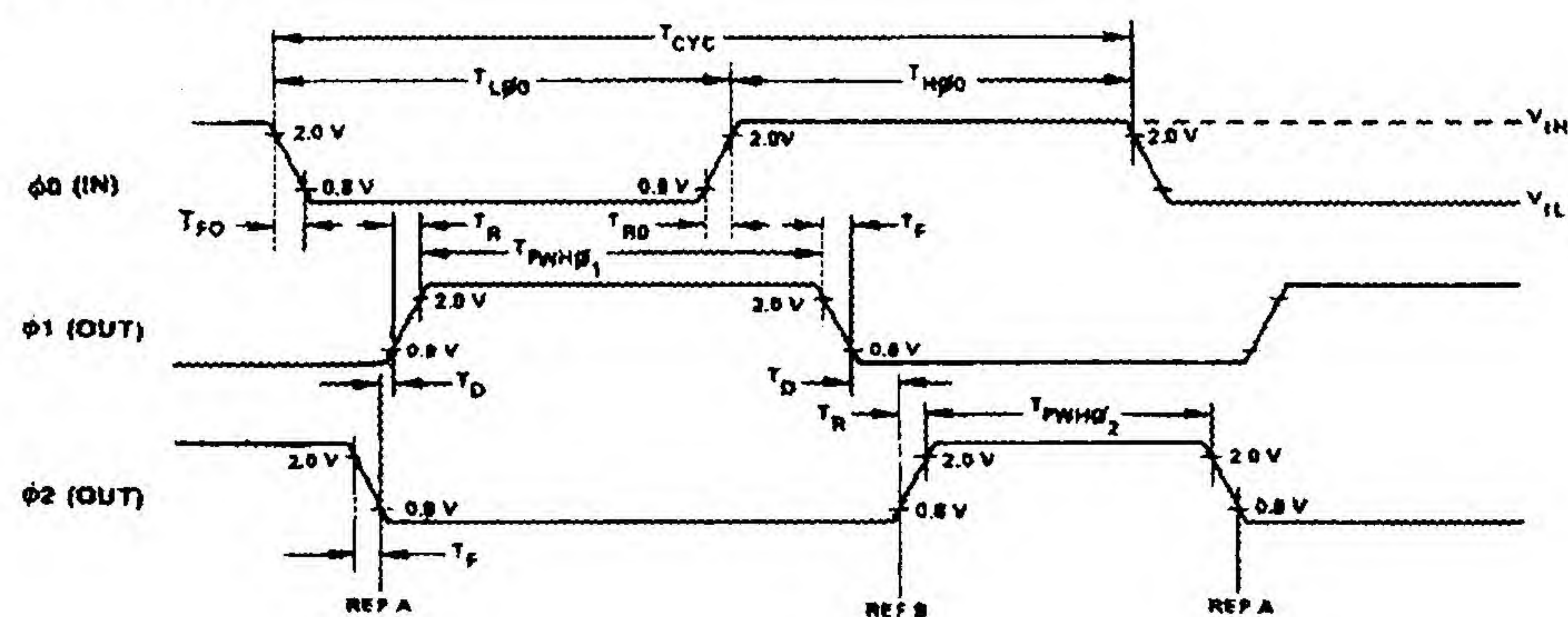
0	BRK	—OP Code
0	Implied	—Addressing Mode
1	7	—Instruction Bytes; Machine Cycles

*Add 1 to N if page boundary is crossed.
 **Add 1 to N if branch occurs to same page;
 add 2 to N if branch occurs to different page.

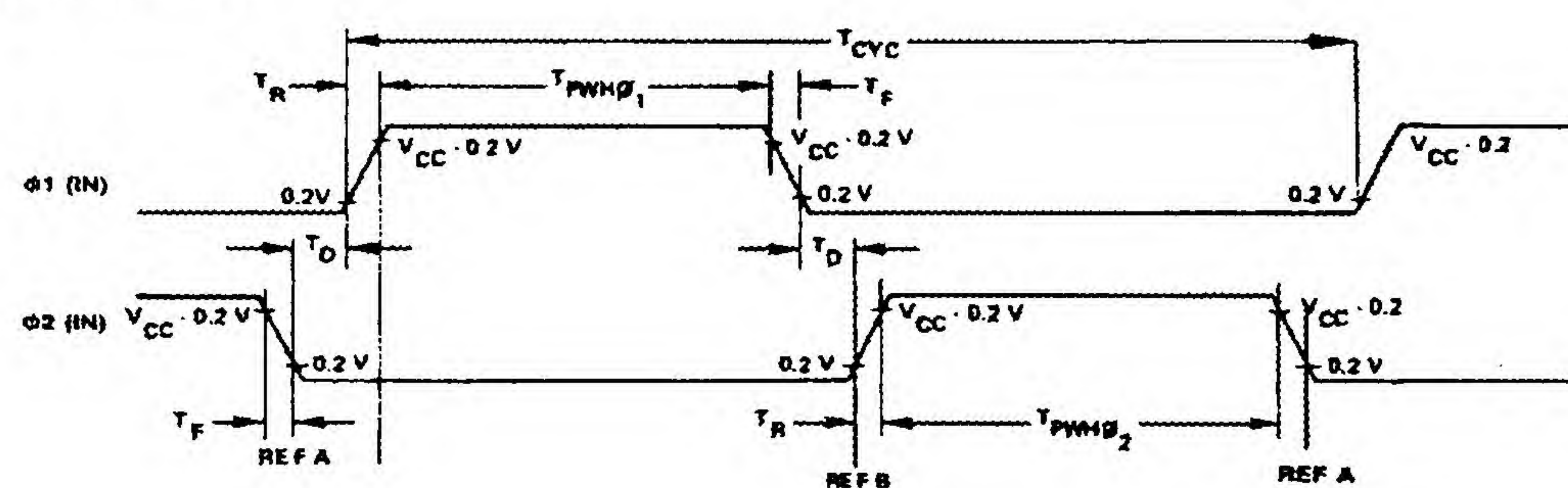
INSTRUCTION SET SUMMARY

INSTRUCTIONS		IMMEDIATE		ABSOLUTE		ZERO PAGE		ACCUM		IMPLIED		IND: X		IND: Y		Z PAGE		ABS X		ABS Y		RELATIVE		INDIRECT		Z PAGE		PROCESSOR STATUS CODES										Mnemonic																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																														
Mnemonic	OPERATION	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	OP	n	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479	480	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510	511	512	513	514	515	516	517	518	519	520	521	522	523	524	525	526	527	528	529	530	531	532	533	534	535	536	537	538	539	540	541	542	543	544	545	546	547	548	549	550	551	552	553	554	555	556	557	558	559	560	561	562	563	564	565	566	567	568	569	570	571	572	573	574	575	576	577	578	579	580	581	582	583	584	585	586	587	588	589	590	591	592	593	594	595	596	597	598	599	600	601	602	603	604	605	606	607	608	609	610	611	612	613	614	615	616	617	618	619	620	621	622	623	624	625	626	627	628	629	630	631	632	633	634	635	636	637	638	639	640	641	642	643	644	645	646	647	648	649	650	651	652	653	654	655	656	657	658	659	660	661	662	663	664	665	666	667	668	669	670	671	672	673	674	675	676	677	678	679	680	681	682	683	684	685	686	687	688	689	690	691	692	693	694	695	696	697	698	699	700	701	702	703	704	705	706	707	708	709	710	711	712	713	714	715	716	717	718	719	720	721	722	723	724	725	726	727	728	729	730	731	732	733	734	735	736	737	738	739	740	741	742	743	744	745	746	747	748	749	750	751	752	753	754	755	756	757	758	759	760	761	762	763	764	765	766	767	768	769	770	771	772	773	774	775	776	777	778	779	780	781	782	783	784	785	786	787	788	789	790	791	792	793	794	795	796	797	798	799	800	801	802	803	804	805	806	807	808	809	810	811	812	813	814	815	816	817	818	819	820	821	822	823	824	825	826	827	828	829	830	831	832	833	834	835	836	837	838	839	840	841	842	843	844	845	846	847	848	849	850	851	852	853	854	855	856	857	858	859	860	861	862	863	864	865	866	867	868	869	870	871	872	873	874	875	876	877	878	879	880	881	882	883	884	885	886	887	888	889	890	891	892	893	894	895	896	897	898	899	900	901	902	903	904	905	906	907	908	909	910	911	912	913	914	915	916	917	918	919	920	921	922	923	924	925	926	927	928	929	930	931	932	933	934	935	936	937	938	939	940	941	942	943	944	945	946	947	948	949	950	951	952	953	954	955	956	957	958	959	960	961	962	963	964	965	966	967	968	969	970	971	972	973	974	975	976	977	978	979	980	981	982	983	984	985	986	987	988	989	990	991	992	993	994	995	996	997	998	999	1000	1001	1002	1003	1004	1005	1006	1007	1008	1009	1010	1011	1012	1013	1014	1015	1016	1017	1018	1019	1020	1021	1022	1023	1024	1025	1026	1027	1028	1029	100

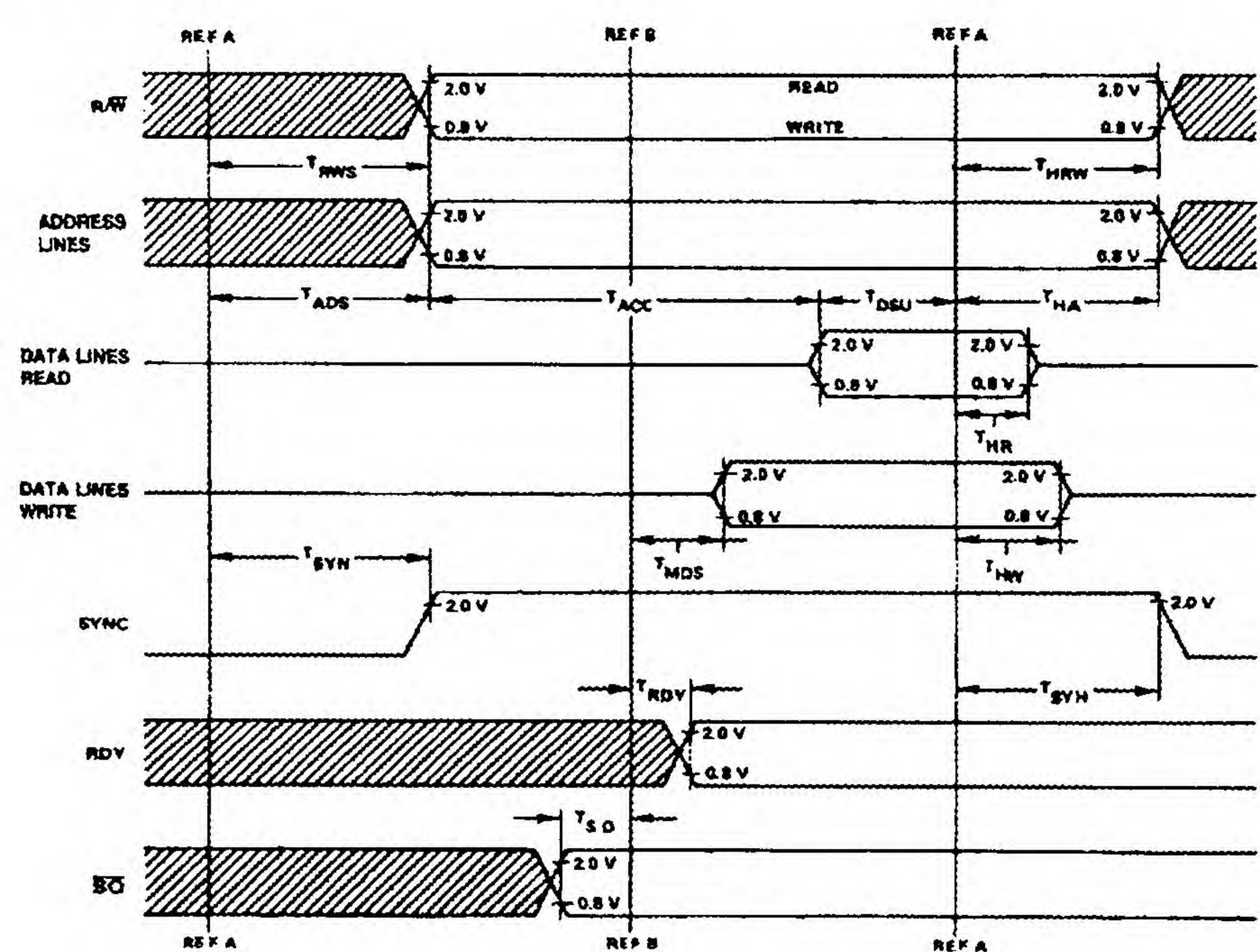
R650X CLOCK TIMING



R651X CLOCK TIMING



R65XX READ WRITE TIMING



AC CHARACTERISTICS

Characteristic	Symbol	R65XX (1 MHz)		R65XXA (2 MHz)		R65XXB (3 MHz)		Unit
		Min	Max	Min	Max	Min	Max	

R650X CLOCK TIMING

Clock Cycle Time	T_{CYC}	1.0	10	0.5	10	0.33	10	μs
$\phi 0$ (IN) Low Pulse Width	$T_{L\phi 0}$	480	—	240	—	160	—	ns
$\phi 0$ (IN) High Pulse Width	$T_{H\phi 0}$	460	—	240	—	160	—	ns
$\phi 0$ (IN) Rise and Fall Time ^{1, 2}	$T_{R\phi 0}, T_{F\phi 0}$	—	10	—	10	—	10	ns
$\phi 1$ (OUT) High Pulse Width	$T_{PWH\phi 1}$	460	—	235	—	155	—	ns
$\phi 2$ (OUT) High Pulse Width	$T_{PWH\phi 2}$	460	—	240	—	160	—	ns
Delay Between $\phi 1$ (OUT) and $\phi 2$ (OUT)	T_D	0	—	0	—	0	—	ns
$\phi 1$ (OUT), $\phi 2$ (OUT) Rise and Fall Time ^{1, 2}	T_R, T_F	—	25	—	25	—	15	ns

R651X CLOCK TIMING

Clock Cycle Time	T_{CYC}	1.0	10	0.5	10	0.33	10	μs
$\phi 1$ (IN) High Pulse Width	$T_{PWH\phi 1}$	430	—	215	—	150	—	ns
$\phi 2$ (IN) High Pulse Width	$T_{PWH\phi 2}$	470	—	235	—	160	—	ns
Delay Between $\phi 1$ and $\phi 2$	T_D	0	—	0	—	0	—	ns
$\phi 1$ (IN), $\phi 2$ (IN) Rise and Fall Time ^{1, 3}	T_R, T_F	—	25	—	20	—	15	ns

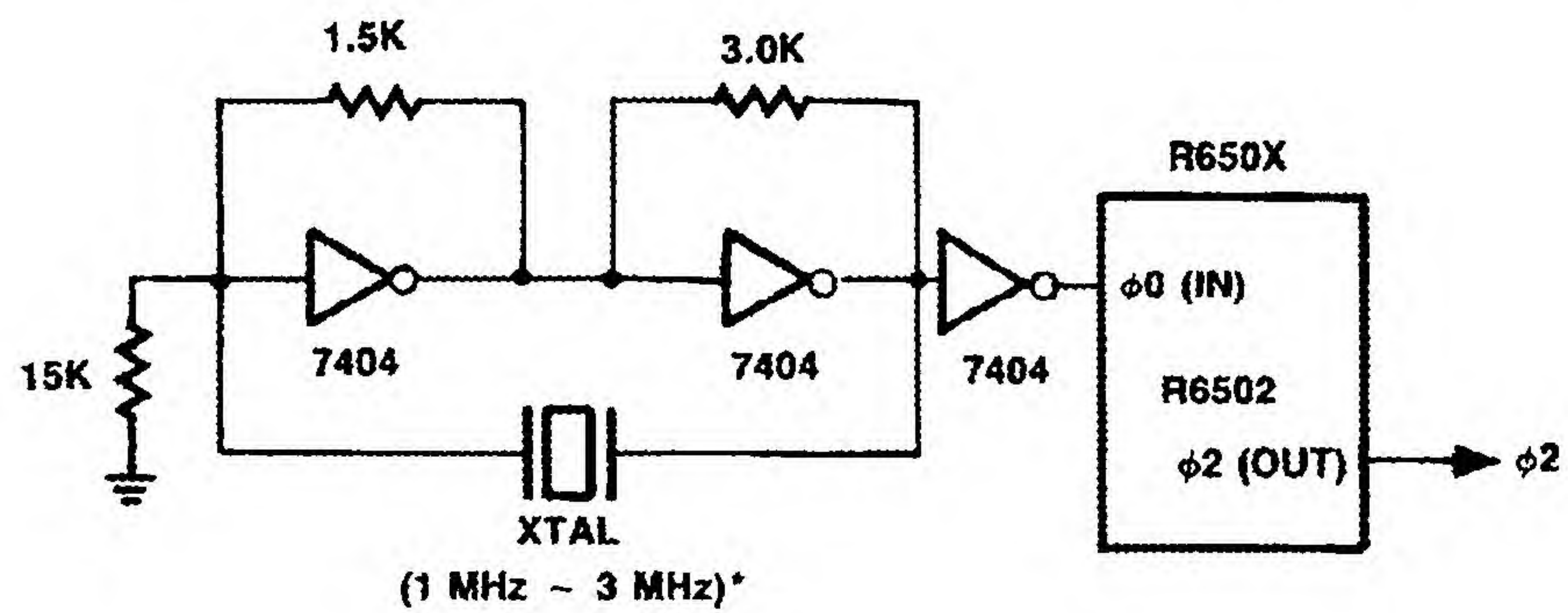
R65XX READ/WRITE TIMING

R/W Setup Time	T_{RWS}	—	225	—	140	—	110	ns
R/W Hold Time	T_{HRW}	30	—	30	—	15	—	ns
Address Setup Time	T_{ADS}	—	225	—	140	—	110	ns
Address Hold Time	T_{HA}	30	—	30	—	15	—	ns
Read Access Time	T_{ACC}	—	650	—	310	—	170	ns
Read Data Setup Time	T_{DSU}	100	—	50	—	50	—	ns
Read Data Hold Time	T_{HR}	10	—	10	—	10	—	ns
Write Data Setup Time	T_{MDS}	—	175	—	100	—	85	ns
Write Data Hold Time	T_{HW}	30	—	30	—	15	—	ns
SYNC Hold Time	T_{SYH}	30	—	30	—	15	—	ns
RDY Setup Time	T_{RDY}	100	—	50	—	35	—	ns
$\overline{S0}$ Setup Time	T_{S0}	100	—	50	—	35	—	ns
SYNC Setup Time	T_{SYN}	—	225	—	140	—	110	ns

Notes:

1. Loads: All output except clocks = 1 TTL + 130 pF. Clock outputs = 1 TTL + 30 pF.
2. Measured between 0.8 and 2.0 points on waveform load.
3. Measured between 10% and 90% points on waveforms.
4. *RDY must never switch states within R_{RDY} to end of $\phi 2$.

EXAMPLE OF TIME BASE GENERATION FOR R6502



*CRYSTAL: CTS KNIGHTS MP SERIES, OR EQUIVALENT

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to +7.0	Vdc
Operating Temperature Range Commercial Industrial	T_A	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

*NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Value
Supply Voltage	V_{CC}	5V \pm 5%
Temperature Range Commercial Industrial	T_A	0°C to +70°C -40°C to +85°C

DC CHARACTERISTICS

($V_{CC} = 5.0V \pm 5\%$, $V_{SS} = 0$; $T_A = T_L$ to T_H , unless otherwise noted)

Parameter	Symbol	Min.	Typ. ⁵	Max.	Unit ¹	Test Conditions
Input High Voltage Logic Ø0 (IN) Ø1 (IN), Ø2 (IN)	V_{IH}	2.0 2.4 $V_{CC} - 0.3$	— — —	V_{CC} V_{CC} $V_{CC} + 0.25$	V	
Input Low Voltage Logic Ø0 (IN), Ø1 (IN), Ø2 (IN)	V_{IL}	-0.3 -0.3	— —	0.8 0.4	V	
Input Leakage Current Logic (Excl. RDY, \overline{SO}) Ø1 (IN), Ø2 (IN) Ø0 (IN)	I_{IN}	— — —	— — —	2.5 100 10	µA	$V_{IN} = 0V$ to 5.25V $V_C = 0V$
Input Leakage Current for Three State Off D0-D7	I_{TSi}	—	—	10	µA	$V_{IN} = 0.4V$ to 2.4V $V_{CC} = 5.25V$
Output High Voltage SYNC, D0-D7, A0-A15, $\overline{R/W}$, Ø1 (OUT), Ø2 (OUT)	V_{OH}	+2.4	—	—	V	$I_{LOAD} = -100 \mu A$ $V_{CC} = 4.75V$
Output Low Voltage SYNC, D0-D7, A0-A15, $\overline{R/W}$, Ø1 (OUT), Ø2 (OUT)	V_{OL}	—	—	+0.4	V	$I_{LOAD} = 1.6 \text{ ma}$ $V_{CC} = 4.75V$
Power Dissipation 1 and 2 MHz 3 MHz	P_D	— —	450 500	700 800	mW	
Capacitance Logic D0-D7 A0-A15, $\overline{R/W}$, SYNC Ø0 (IN) Ø1 (IN) Ø2 (IN)	C C_{IN} C_{OUT} $C_{Ø0(IN)}$ $C_{Ø1}$ $C_{Ø2}$	— — — — — —	— — — — 30 50	10 15 12 15 50 80	pF	$V_{CC} = 5.0V$ $V_{IN} = 0V$ $f = 1 \text{ MHz}$ $T_A = 25^\circ C$

Notes:

1. All units are direct current (dc) except for capacitance.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. \overline{IRQ} and \overline{NMI} require 3K pull-up resistor.
4. Ø1 (IN) and Ø2 (IN) apply to R6512, 13, 14, and 15; Ø0 (IN) applies to R6502, 03, 04, 05, 06 and 07.
5. Typical values shown for $V_{CC} = 5.0V$ and $T_A = 25^\circ C$.

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